

Applicant(s): Soo-geun Lee, et al.
U.S. Serial No.: 10/081,661

REMARKS

Claims 1-8 and 18 are rejected under 35 U.S.C. §103(a) as being unpatentable over Lui (U.S. Patent Number 6,391,761) in view of Bothra, et al. (U.S. Patent Number 6,221,759). Claims 9, 10 and 14 are rejected under 35 U.S.C. §103(a) as being unpatentable over Liu in view of Bothra, as applied to claims 1-8, and further in view of Nashner, et al. (U.S. Patent Number 6,465,358). Claims 11-13 and 15-17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Liu in view of Bothra, as applied to claims 1-8 and 18, and further in view of Liu, et al. (U.S. Patent Number 6,323,121). In view of the amendments to the claims and the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

The applicants' invention is directed to a dual damascene process used in forming an interconnection line in a semiconductor device. A first etch stopper is formed on a lower conductive layer that is formed in a semiconductor substrate. A first interlayer insulating layer is formed on the first etching stopper, and a second etching stopper is formed on the first interlayer insulating layer. A second interlayer insulating layer is formed on the second etching stopper. The second interlayer insulating layer, the second etching stopper and the first interlayer insulating layer are etched to form a via hole aligned with the lower conductive layer. During this etching, the first etching stopper is used as an etching stopping point. After the via is formed, a protective layer is formed in the via to protect a portion of the first etching stopper exposed at the bottom of the via hole. A portion of the second interlayer insulating layer is then etched using the second etching stopping layer as an etching stopping point such that a trench is formed connected to the via hole. The protective layer is then removed, and the portion of the first etching stopper at the bottom of the via hole is removed. An upper conductive layer filling the via hole and trench is then formed.

In accordance with the invention, the protective layer fills the via hole such that when the second interlayer insulating layer is etched to form the trench, the etching does not adversely affect the first etching stopper at the bottom of the via hole. This prevents damage to the lower

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conductive layer during the etch.

The claims have been amended to specifically recite features of the invention. That is, the claims are amended to clarify that the protective layer fills the via hole. It is believed that this clarifying claim language serves to distinguish the cited prior art.

In Liu, the liner layer 78 is formed in the via hole to maintain integrity of the via profile during subsequent etching. As stated at column 4 lines 50-61, the purpose of the liner layer is to protect the vertical side walls of the via trenches during the metal conductivity layer etch. That is, the liner layer 78 is used to prevent the faceting problem of the prior art illustrated in Figure 3 of Liu. It is not used to protect a portion of an etching stopper exposed at the bottom of the via hole, as claimed by the applicants. Since the purpose of the liner layer 78 in Liu is to protect the vertical side walls, instead of the bottom of the via hole, it need not fill the via hole. This is in contrast to the applicants' device set forth in the amended claims in which the protective layer fills the via hole.

Accordingly, Liu fails to teach or suggest the invention set forth in the amended claims. That is, Liu fails to teach or suggest a protective layer filling a via hole to protect a portion of a first etching stopper exposed at the bottom of the via hole. Bothra is cited as teaching the via hole aligned with the lower conductive layer. However, Bothra does not provide teaching or suggestion of a protective layer filling a via hole to protect a portion of a first etching stopper exposed at the bottom of the via hole.

Since neither Liu nor Bothra teaches or suggests the protective layer filling a via hole to protect the first etching stopper exposed at the bottom of the via hole, combining the references fails to provide such teaching or suggestion. Therefore, Liu and Bothra, taken alone or in combination, fail to teach or suggest the invention set forth in the amended claims. Accordingly, it is believed that the claims are allowable over the references, and reconsideration of the rejections of claims 1-8 and 18 under 35 U.S.C. §103(a) based on Liu and Bothra is respectfully requested.

Nashner, et al. is cited as teaching a spin-on type dielectric protective layer and removal of the protective layer using a wet-etching technique with HF solution diluted with water. However, Nashner, et al. fails to teach or suggest the protective layer filling the via hole to protect the first etching stopper exposed at the bottom of the via hole. Accordingly, combining

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Nashner, et al. with Liu and Bothra fails to result in the applicants claimed invention. Therefore, it is believed that the claims are allowable over Liu, Bothra and Nashner, et al., and reconsideration of the rejections of claims 9, 10 and 14 under 35 U.S.C. §103(a) based on Liu, Bothra and Nashner, et al. is respectfully requested.

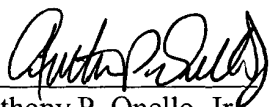
Liu, et al. is cited as disclosing the claimed details regarding the formation of the protective layer. However, Liu, et al. also fail to teach or suggest the protective layer filling the via hole to protect the first etching stopper exposed at the bottom of the via hole. Accordingly, combining Liu, et al. with Liu and Bothra fails to result in teaching or suggesting that feature set forth in the amended claims. Therefore, it is believed that the claims are allowable over Liu, Bothra and Liu, et al., and reconsideration of the rejections of claims 11-13 and 15-17 under 35 U.S.C. §103(a) based on Liu, Bothra and Liu, et al. is respectfully requested.

Attached hereto is a marked-up version of the changes made to the application by the current Amendment. The attached pages are captioned "Version with Markings to Show Changes Made."

In view of the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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Version with Markings to Show Changes Made

In the Claims

Claim 1 has been amended as follows:

1. (Amended) A method of forming an interconnection line in a semiconductor device comprising:
 - forming a first etching stopper on a lower conductive layer which is formed on a semiconductor substrate;
 - forming a first interlayer insulating layer on the first etching stopper;
 - forming a second etching stopper on the first interlayer insulating layer;
 - forming a second interlayer insulating layer on the second etching stopper;
 - etching the second interlayer insulating layer, the second etching stopper, and the first interlayer insulating layer sequentially using the first etching stopper as an etching stopping point to form a via hole aligned with the lower conductive layer;
 - forming a protective layer to protect a portion of the first etching stopper exposed at the bottom of the via hole, the protective layer filling the via hole;
 - etching a portion of the second interlayer insulating layer adjacent to the via hole using the second etching stopper as an etching stopping point to form a trench connected to the via hole;
 - removing the protective layer;
 - removing the portion of the first etching stopper positioned at the bottom of the via hole; and
 - forming an upper conductive layer that fills the via hole and the trench and is electrically connected to the lower conductive layer.